TECHNISCHE UNIVERSITÄT DRESDEN
Institute of Electromechanical and Electronic Design
www.ifte.de

MICROPLAN:
Micro-System Design and Production-Planning Tool

Tilman Horst, Robert Fischbach and Jens Lienig

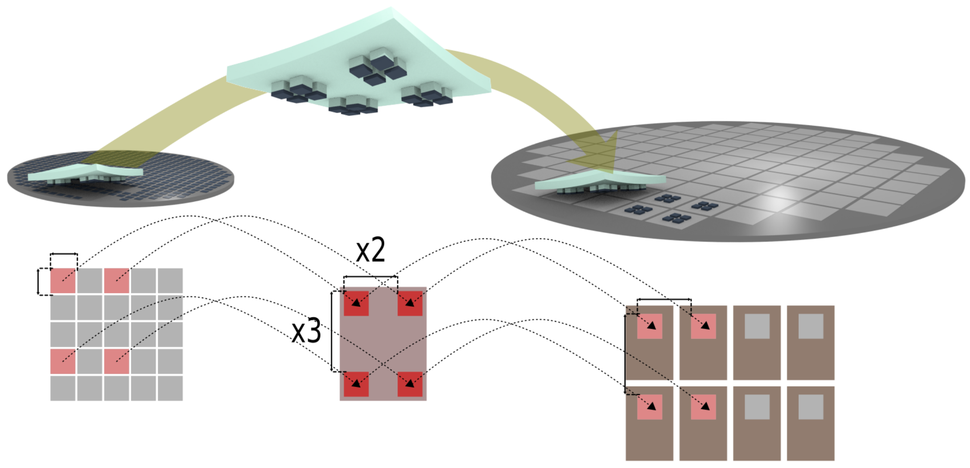
Outline

Heterogeneous systems combine components stemming from different manufacturing processes in one package. As such, they provide a wide range of opportunities for next generation automotive sensors, biosensors, silicon photonics, integrated power electronics and more. However, while many of these applications proved their feasibility in laboratory environments, industrial application is lagging behind due to high manufacturing costs.
Micro-transfer printing is a manufacturing technology for heterogeneous systems that uses a micro-structured elastomer stamp to manufacture systems consisting of multiple dies. The main features are:

- **Massive parallelization of die transfer to reduce processing time and cost**
- **Transfer between wafers of different sizes (e.g. 6-inch to 8-inch)**
- **Transfer of dies of different sizes**

Here, we present a package-layout tool which enables users to design cost-optimized layouts compliant with the micro-transfer printing process (µTP). It is developed in close cooperation with X-Fab within the MICROPRINCE project. For further information on the project, visit https://microprince.eu/.

Wafer and Stamp Compatibility

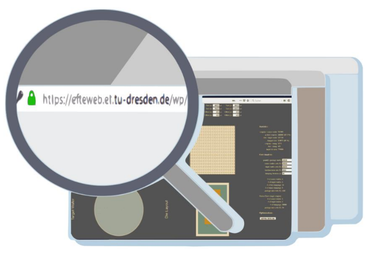


To make use of the transfer-printing process, the wafers and the stamp need to be compatible. For optimal results, the target pitch has to be an integer multiple (1, 2, 3, …) of the source pitch. Also other proportions are possible, but require larger stamps and thus reduce the wafer utilization.

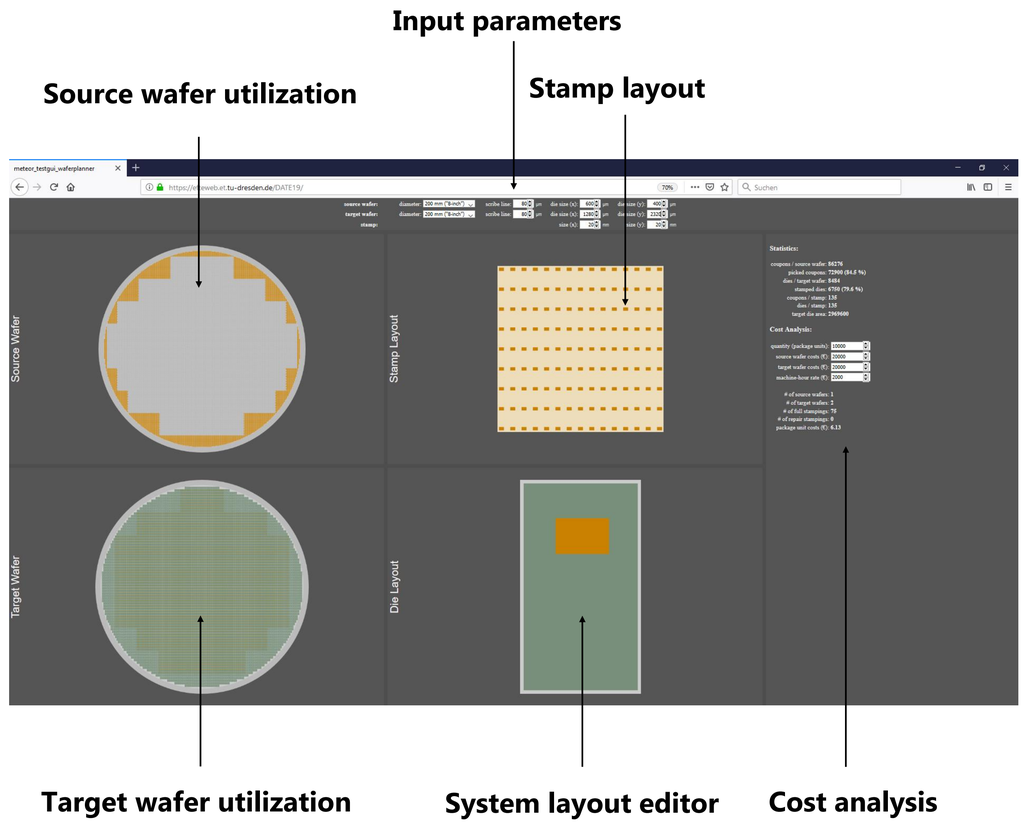
How to Get the Tool

No installation is required to run the tool. Just open an internet browser and type the URL or scan the QR Code with your smartphone/ tablet. When asked, provide the username and password below.

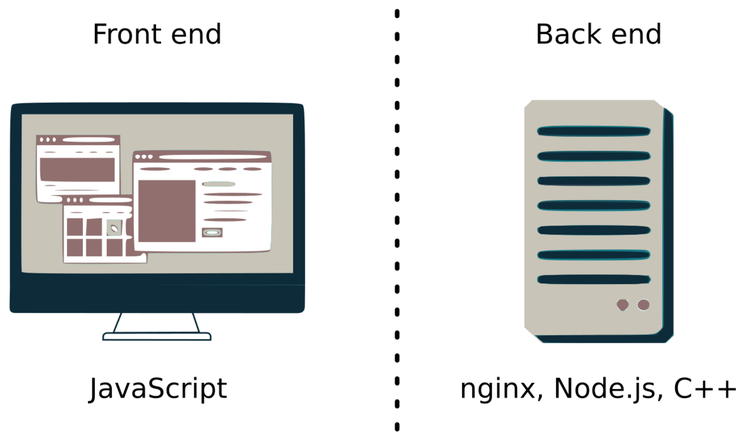
URL: https://efteweb.et.tu-dresden.de/DATE19/
Username: UniversityBooth
Password: DATE2019



User Interface

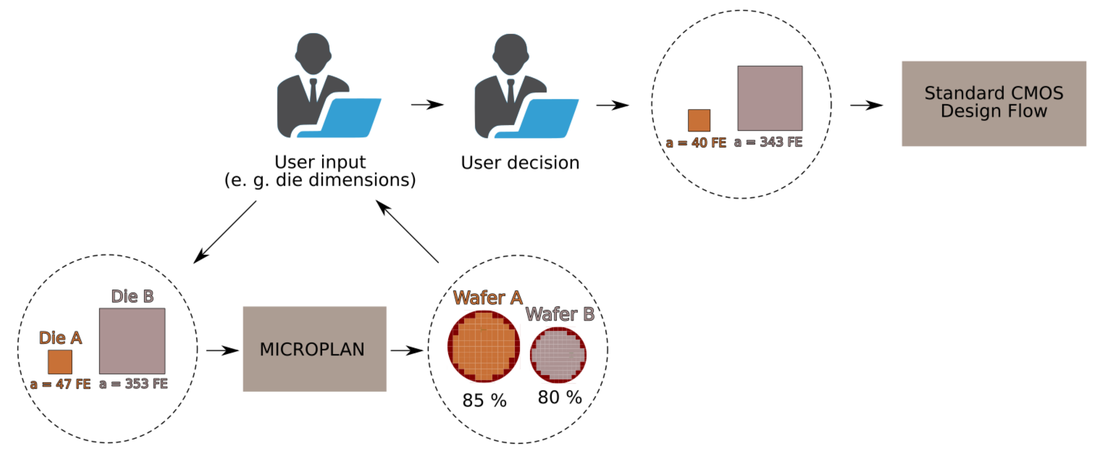


Implementation



For parameter input, we use a JavaScript font end on the client side. At the back end, we use C++ code for determining the wafer utilization. For more information on the back end refer to [1].

Design Flow Integration



The tool is easily integrated into existing standard CMOS design flows. The user can input desired parameters (e. g. die dimensions) and will get the resulting wafer utilizations. In case of unsatisfying results, the input can be varied until a more satisfactory result is reached. The determined dimensions can eventually be used as input in a standard CMOS flow.

[1] Robert Fischbach et al., Assembly-Related Chip/Package Co-Design of Heterogeneous Systems Manufactured by Micro-Transfer Printing, Proceedings of the DATE Conference, 2019.
This work has received funding from the European Union's H2020 Program (ECSEL) under grant agreement number 737465, from the BMBF of Germany and from the SMWA of the FreistaatSachsen under grant agreement number 16ESE0231S (project “Microprince”).

Postal Address
Technische Universitaet Dresden
Institut fuer Feinwerktechnik und Elektronik-Design
01062 Dresden, Germany

Visitors
Helmholtzstraße 18
01069 Dresden, Germany
Barkhausenbau BAR II/20 D

Website
www.ifte.de